REMARKS

The applicants appreciate the Examiner's thorough examination of the Application and request reexamination and reconsideration of the Application in view of the following remarks.

The Examiner has objected to the drawings, asserting that they fail to indicate the third switch claimed in claim 7. Applicants herein amend claim 7 to remove the reference to the third switch. This amendment is not made for reasons related to patentability because it merely corrects a typographical error. Applicants respectfully request that the Examiner withdraw the objection to the drawings.

Claims 1-23 stand rejected under 35 U.S.C. §112 as allegedly being indefinite. Applicants herein amend claim 1 to recite that the integrating switch capacitor circuit includes the summing junction. This amendment is not made for reasons related to patentability because it does not change the scope of the claim.

The Examiner indicates that claims 7-8, 10-12 and 17 would be allowable if rewritten to overcome the rejections under 35 U.S.C. §112, 2nd paragraph, and if rewritten to include all the limitations of the base claim and any intervening claims. Applicants herein add new claims 24-29 which correspond to allowed claims 7-8, 10-12 and 17. Applicants would like to thank the Examiner for the indication of allowable subject material.

Claims 1, 14 and 15 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent No. 5,914,638 to He.

Applicants herein amend claim 1 to better define the invention. Specifically, Applicants amend claim 1 to recite that the offset capacitor of the correlated double

sampling capacitor circuit stores the voltage offset of the summing junction in one cycle and subtracts the voltage offset from the output of the integrating capacitor in another cycle. Support for this amendment is found at page 7, lines 7-9.

The subject invention results from the realization that an improved switched capacitor integrator system with reduced gain problems, reduced offset errors, and higher linearity and resolution amplifier output voltage can be effected by applying an input cascoded amplifier architecture to reduce Miller capacitance for correlated double sampling to form an integrator, even in light of multiple inputs and functions. In addition, this particular implementation of CDS, its interconnections with coexisting circuit elements, works more effectively to make the new summing junction more stable and hence improve the linearity and resolution of the amplifier outputs. See the subject application at page 3, lines 9-16.

Cascode amplifiers are an often used type of amplifier because they provide high gain. The subject invention results from the recognition that correlated double sampling can be done much more effectively using cascode amplifiers not for high gain reasons but rather an amplifier with the input differential pair cascoded effectively <u>eliminates Miller capacitive effects</u> from the input to the output of the input transistors thus maintaining better stability of the summing junction SJ, node 56, Fig. 5. See the subject application at page 11, lines 9-14.

In contrast to the subject invention, He relates to an apparatus for adjusting the output voltage of a sample-and-hold amplifier. As shown in Fig. 3 of He, sample-and-hold amplifier 60 includes cascode amplifier circuit AMP1, sampling circuit 74, and feedback circuit 100. Sampling circuit 74 includes integrating capacitors C1-C4,

switches SW1-SW6 and switches SW10-SW12. In paragraph 3 of the Office Action, the Examiner asserts that sampling circuit 74 of He reads on both the integrated switch capacitor circuit and the correlated double sampling capacitor circuit as claimed by Applicants. However, He fails to teach, disclose or suggest a correlated double sampling capacitor circuit that stores the voltage offset of the summing junction in one cycle and subtracts the voltage offset from the output of an integrating capacitor in another cycle.

Rather, He merely discloses sampling circuit 74 for sampling the input voltage on lines 70 and 72. For example, Fig. 4 of He shows a first state when switches SW1-SW6 are closed and switches SW10 and SW12 are left open. In this state, the voltages on input lines 70 and 72 charge the capacitors C1-C4 relative to the voltage on reference input 85. Fig. 5 shows a second state in which switches SW1-SW6 are open. In this second state, capacitors C2 and C3 are used as sampling capacitors for transferring the sample charges to the inputs of amplifier AMP1. Capacitors C1 and C4 are used as integrating capacitors for the operational amplifier AMP1. Clearly, Figs. 3-5 relate to a sample-and-hold amplifier rather than an <u>integrating switch capacitor circuit</u> and a <u>correlated double sampling capacitor circuit</u> as claimed by Applicants.

Accordingly, He fails to teach, disclose or suggest the claimed invention of Applicants' claim 1. Applicants respectfully request that the Examiner withdraw this rejection.

Claims 1-5, 13-14, 16 and 18-23 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over either U.S. Patent No. 4,893,088 to Myers et al., U.S. Patent No. 5,479,130 to McCartney, or U.S. Patent No. 5,391,999 to Early et al., all in view of He; claims 1-6, 13-14, 16 and 18-23 stand rejected under 35 U.S.C. §103(a) as

allegedly being unpatentable over either U.S. Patent No. 4,894,620 to Nagaraj or Nagaraj et al. in *Electronics Letter* (1985), in view of He; claims 1-5, 9, 13-14, 16 and 18-23 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 6,469,561 to Pernigotti et al. in view of He.

The Examiner admits that each of the references besides He fails to disclose a cascoded amplifier circuit. To overcome the deficiencies of each of these references, the Examiner combines He with each of these references. The Examiner alleges in the Office Action that the motivation for using a cascoded amplifier is to obtain the advantages allegedly associated with such a circuit, i.e., lowered capacitance and improved frequency response. As described below, however, none of these remaining references, or He itself, teach or suggest combining any of these references together to provide Applicants' claimed invention. Moreover, none of the cited references describe the problem of overcoming Miller capacitance when a correlated double sampling capacitor circuit is used, as does the subject application.

Myers et al. relates to a transimpedance focal plane processor that includes amplifier A1, input integrator 10, sample and hold and low-pass filter 14, and feedback integrator 16. The Examiner asserts that capacitor C2 is an offset capacitor. However, Myers et al. fails to teach, disclose or suggest Applicants' claimed correlated double sampling capacitor circuit that includes <u>an offset capacitor interconnected between a summing junction and an input of a cascoded amplifier circuit</u>. Rather, Myers et al. discloses that capacitor C2 is connected between switch 12 and capacitor C4 instead of between a summing junction and an <u>amplifier circuit</u> as claimed by Applicants. In fact, capacitor C1 of Myers et al. is only a typical integrating capacitor C1 connected between

the input and output of amplifier A1. Thus, Myers et al. fails to teach, disclose or suggest the correlated double sampling capacitor circuit as claimed by Applicants.

Moreover, Myers et al. does not teach, disclose or suggest the desirability of using an input cascoded amplifier circuit. Rather, Myers et al. discloses only the use of operational amplifiers A1, A2 and A3 and thus does not teach the desirability of input cascoded amplifiers.

McCartney relates to an auto-zero switched-capacitor integrator that includes CMOS operational amplifier 12. McCartney does not teach, disclose or suggest the desirability of using an input cascoded amplifier circuit. Rather, McCartney only promotes the use of CMOS operational amplifiers. Specifically, McCartney describes that:

> Switched-capacitor circuits have widespread use due to the advancement of CMOS technology. CMOS technology is commonly used to implement switched-capacitor circuits because of the availability of MOSFET switches and op amps with low input bias currents. One common type of switched-capacitor circuit is a switched-capacitor integrator. CMOS switched-capacitor integrator circuits are commonly used in sigma delta analog-to-digital converters. Such CMOS switched-capacitor integrator circuits typically include switches, capacitors and op amps.

McCartney at Col. 1, lines 13-22. Thus, McCartney does not teach the desirability of input cascoded amplifiers.

Early et al. relates to a glitchless switched-capacitor biquad low pass filter. Early et al. discloses the use of operational amplifiers 12 and 28 in Fig. 1, operational amplifiers 47 and 69 in Fig. 2, and operational amplifiers 90 and 106 in Fig. 3. Early et al. does not teach the desirability of an input cascoded amplifier circuit, rather it

teaches that its circuits in Figs. 2 and 3, which do not include input cascoded amplifiers, are sufficient to provide glitchless operation of the switched-capacitor biquad low pass filters of Figs. 2 and 3.

Likewise, Nagaraj, which relates to a switched capacitor circuit, does not teach, disclose or suggest the use of an input cascoded amplifier circuit. Rather, Nagaraj only discloses the use of operational amplifier A1 in Figs. 1-4, and shows undescribed amplifiers in Figs. 5-9.

Electronics Letters, which relates to switched capacitor filters, provides no description of its operational amplifier A1. *Electronics Letters*, however, does teach that the use of a non-standard op-amp is undesirable. *See Electronics Letters* at Col. 3, lines 1-3. Thus, *Electronics Letters* specifically <u>teaches away</u> from using a non-standard operational amplifier, such as an input cascoded amplifier circuit, as claimed by Applicants.

Pernigotti et al. relates to a rail to rail rectifying integrator. Pernigotti et al. shows operational amplifiers in Figs. 2a, 3b and 5. However, Pernigotti et al. fails to teach, disclose or suggest the desirability of an input cascoded amplifier circuit. In fact, Pernigotti et al. fails to disclose any teaching of the type of the operational amplifier shown in its figures and does not even label the operational amplifier shown in Fig. 5, which the Examiner cites. Thus, Pernigotti clearly does not teach the use of an input cascoded amplifier circuit, as claimed by Applicants.

Thus, the Examiner has failed to provide any teaching, motivation or suggestion in the references themselves, or in the prior art, that such a combination would be desirable. In particular, <u>none of these references relate to or describe overcoming the</u>

effect of Miller capacitance from using correlated double sampling as does the subject application. Without the description of the problem of Miller capacitance due to the use of correlated double sampling, there is no motivation to overcome the problem by using an input cascoded amplifier circuit, as does the invention as claimed by Applicants. Thus it is clear that the only such motivation to use an input cascoded amplifier circuit with the integrated switched capacitor circuit and the correlated double sampling capacitor circuit of the subject invention comes from Applicants' own application, and it is improper for the Examiner to use hindsight construction to arrive at Applicants' claimed invention.

Claim 1 of the subject invention recites: "[a] switched capacitor integrator system comprising: an input cascoded amplifier circuit; an integrating switched capacitor circuit including an integrating capacitor and a summing junction, said integrating switched capacitor circuit connected to the output of said cascoded amplifier circuit and to said summing junction; said integrating switched capacitor circuit including an input switched capacitor circuit responsive to an input and connected to said summing junction; and a correlated double sampling capacitor circuit including an offset capacitor interconnected between said summing junction and an input of said cascoded amplifier circuit, the offset capacitor storing an offset voltage of the summing junction in one cycle, and subtracting the offset voltage from the output of the integrating capacitor in another cycle."

As noted above, He fails to disclose a correlated double sampling capacitor circuit as claimed by Applicants and does not relate to the subject invention as claimed by Applicants. All of the cited references, either alone or in combination, fail to teach, disclose or suggest an input cascoded amplifier circuit and none of these references, nor the knowledge available to those skilled in the art, provide the teaching, suggestion or

motivation to combine an input cascoded amplifier circuit with an integrated switched capacitor circuit and a correlated double sampling capacitor circuit. In fact, some of these references actually teach away from combining an input cascoded amplifier circuit with an integrating switch capacitor circuit.

Accordingly, claims 1-23 are allowable over the cited references. Applicants respectfully request that the Examiner withdraw the above rejections to these claims.

Each of the Examiner's rejections have been addressed or traversed. Accordingly, it is respectfully submitted that the application is in condition for allowance. Early and favorable action is respectfully requested.

If for any reason this Response is found to be incomplete, or if at any time it appears that a telephone conference with counsel would help advance prosecution, please telephone the undersigned or his associates collect in Waltham, Massachusetts at (781) 890-5678.

Respectfully submitted,

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